IN THE CLAIMS:

Please amend claims 36, 40 and 44-48; cancel claim 49; and add claims 53-63, as set forth below:

1-35. (Canceled)

36. (Currently Amended) A pFET synapse transistor, comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including:

a first n- well;

a first p+ doped region disposed in said first n- well forming a first source;

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased ~~responsive to increase in~~ when a voltage difference between the first source and the first drain is increased; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second

drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and

a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased when ~~increase responsive to increase in~~ voltage at the second drain or the second source is increased, wherein the conductor comprises a conductive layer which forms a bridge over said second polysilicon floating gate.

37-38. (Canceled)

39. (Previously Presented) The pFET synapse transistor in accordance with claim 36, wherein said readout transistor and the shorted transistor include a single layer of conductive polysilicon.

40. (Currently amended) The pFET synapse transistor in accordance with claim 36, wherein the pFET synapse transistor is fabricated using a standard CMOS process.

41-43. (Canceled)

44. (Currently Amended) A pFET synapse transistor, comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including:

a first n- well;

a first p+ doped region disposed in said first n- well forming a first source;

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased ~~responsive to increase in~~ when a voltage difference between the first source and the first drain is increased; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate;

a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased ~~responsive to increase in~~ when voltage at the second drain or the second source is

increased, wherein the conductor comprises a conductive layer which forma s bridge over said second polysilicon floating gate; and

a well contact terminal electrically coupled to said second n- well, wherein said synapse transistor is configured to operate as a current source without gate input using a single polysilicon gate layer.

45. (Currently Amended) A system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip, the system comprising:

a pFET synapse transistor including:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including [[;]]:

a first n- well;

a first p+ doped region disposed in said first n- well forming a first source;

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased ~~responsive to increase in~~ when a voltage difference between the first source and the first drain is increased; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and

a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased ~~responsive to increase in~~ when voltage at the second drain or the second source is increased.

46. (Currently Amended) A p-channel floating-gate device connected to a digital-to-analog converter, comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including:

a first n- well;

a first p+ doped region disposed in said first n- well forming a first source;

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased ~~responsive to increase in~~ when a voltage difference between the first source and the first drain is increased; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and

a conductor connecting the second drain and the second source, a number of electrons removed from the second polysilicon floating gate is increased ~~responsive to increase in~~ when voltage at the second drain or the second source is increased.

47. (Currently Amended) A system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip, the system comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including:

a first n- well;

a first p+ doped region disposed in said first n- well forming a first source;

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased ~~responsive to increase in~~ when a voltage difference between the first source and the first drain is increased; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and

a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased ~~responsive to increase in~~ when voltage at the second drain or the second source is increased.

48. (Currently Amended) A p-channel floating gate device comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including:

a first n- well;

a first p+ doped region disposed in said first n- well forming a first source;

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate is increased when ~~increased responsive to increase in~~ a voltage difference between the first source and the first drain is increased; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and

a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased ~~responsive to increase in~~ when voltage at the second drain or the second source is increased.

49-50. (Canceled)

51. (Previously Presented) The p-channel floating gate device in accordance with claim 48, wherein said readout transistor and the shorted transistor include a single layer of conductive polysilicon.

52. (Previously Presented) The p-channel floating gate device in accordance with claim 48, wherein the floating gate device is fabricated using a standard CMOS process.

53. (New) The pFET synapse transistor in accordance with claim 36, wherein the pFET synapse transistor is configured to trim a current source in a digital-to-analog (DAC) converter.

54. (New) The pFET synapse transistor in accordance with claim 44, wherein the pFET synapse transistor is configured to trim a current source in a digital-to-analog (DAC) converter.

55. (New) The pFET synapse transistor in accordance with claim 44, wherein said readout transistor and the shorted transistor include a single layer of conductive polysilicon.

56. (New) The pFET synapse transistor in accordance with claim 44, wherein the pFET synapse transistor is fabricated using a standard CMOS process.

58. (New) The SOC in accordance with claim 45, wherein the pFET synapse transistor is configured to trim a current source in a digital-to-analog (DAC) converter.

59. (New) The SOC in accordance with claim 45, wherein said readout transistor and the shorted transistor include a single layer of conductive polysilicon.

60. (New) The SOC in accordance with claim 45, wherein the SOC is fabricated using a standard CMOS process.

61. (New) The p-channel floating-gate device in accordance with claim 46, wherein the p-channel floating-gate device is configured trim a current source in a digital-to-analog (DAC) converter.

62. (New) The p-channel floating-gate device in accordance with claim 48, wherein the p-channel floating-gate device is configured trim a current source in a digital-to-analog (DAC) converter.

63. (New) The p-channel floating-gate device in accordance with claim 48, wherein the p-channel floating-gate device is fabricated using a standard CMOS process.